DOCUMENT REVISION STATUS

REV	EO/ECN	CHECK	DATE	ENGR	DATE	REV	EO/ECN	CHECK	DATE	ENGR	DATE
A	14999	H Brown	10/6/80	M. Nasr	10/7/80						
B	15144	S. Nash	11/5/80	M. Nasr	11/26/80						

SHEET REVISION STATUS

SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV
1	B	16	A												
2	B	17	B												
3	B	18	B												
4	B	19	B												
5	B	20	B												
6	B	21	B												
7	A	22	B												
8	B	23	B												
9	B	24	B												
10	A	25	B												
11	B	26	B												
12	B	27	B												
13	B	28	B												
14	B	29	B												
15	B														

ISB 3100 Z80 BASED

PROCESSOR CARD

INTERSIL
275 HAMMERWOOD AVENUE
SUNNYVALE, CA. 94086

TITLE			
SPEC-ISB 3100			
NEXT ASSEMBLY	SYSTEM	DOCUMENT NO.	SHEET
	STD BUS	22-00002	1

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1.0 FEATURES

- Fully buffered signals for system expandability
- Up to 8K bytes EPROM capacity in 2 or 4K bytes increments (two EPROM sockets)
- Up to 4K bytes static RAM capacity in 1K increments
- Jumper selectable (2716 or 2732 EPROMS)
- Full memory decoding capability to map on board EPROM/RAM anywhere in 64K bytes address field in 4K increments
- Full bus arbitration circuitry to arbitrate between: on board memory access/off board memory access, on board I/O operation/ off board I/O operation, on board timer counter interrupt request/ off board interrupt request.
- Four independent timer/counter channels with daisy chain priority interrupt arbitration for all four channels.
- Programmable power on restart to jump anywhere in the address field.
- Power on reset and pushbutton reset input.
- 4 MHz clock frequency
- Jumper selectable external clock input for Z80 processor or any of the timer/counters
- Tri state address, data and control bus
- Single +5V supply
- Optional one wait state during any memory cycle.

2.0 DESCRIPTION

The Intersil ISB 3100 is a Z80 based STD BUS compatible processor module on a 6.5" x 4.48" CARD.

The card contains space for 4K bytes of static RAM in 1K increments utilizing the popular 2114 (1K x4) static RAMS. It also contains two socket locations for EPROMS; either 2716 (2K x 8) or 2732 (4K x 8) can be selected through the jumper strap. Four independent timer/counter channels with interrupting capability and daisy-chain priority arbitration also provided. Other features include 4 MHZ clock frequency, power on reset/pushbutton reset inputs, jumper selectable external clock input for processor or any of the timer/counter channels, fully buffered, 3 state address/data/control signals to the BUS, 4 MHZ clock from card to the BUS and single +5V supply.

The memory mapping for on board RAMS and EPROMS are jumper selectable and can be mapped in 4K blocks anywhere on the 64K memory field in 4K increments. On board RAMS and EPROMS can also be totally bypassed and removed from the board.

BUS arbitration logic ensures proper arbitration between the following operations:

On board memory vs. off board memory.

On board I/O or interrupt acknowledge vs. off board I/O or interrupt acknowledge.

The CPU on power on restart can start at X'0000' or be programmed to jump to any location within the address field. If the latter is chosen, 3 bytes of the first EPROM on the board are to be used to store the jump address. After reading the starting address, the circuitry disables the EPROM or maps it at other pre-assigned locations other than X'0000'.

One wait state can be inserted during any memory cycle to ensure the proper operation of the CPU in conjunction with slower memories. This circuitry can also be disabled; so there would be no wait state.

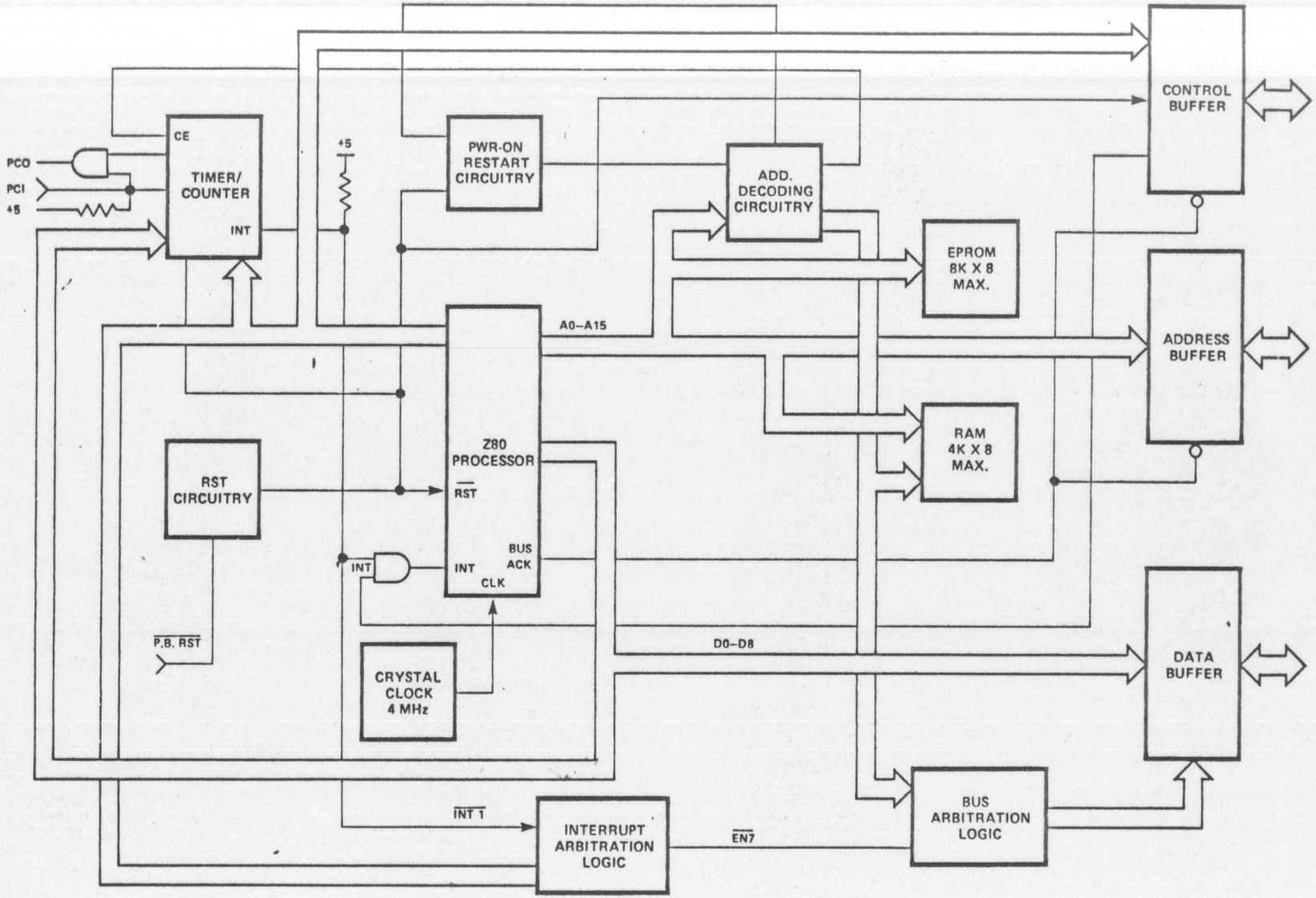

CE
TIMER/
COUNTER
INT
PCO
PCI
+5
+5
PWR-ON
RESTART
CIRCUITRY
ADD.
DECODING
CIRCUITRY
CONTROL
BUFFER
EPROM
8K X 8
MAX.
ADDRESS
BUFFER
A0–A15
Z80
PROCESSOR
RST
BUS
ACK
INT
CLK
RST
CIRCUITRY
RAM
4K X 8
MAX.
INT
P.B. RST
CRYSTAL
CLOCK
4 MHz
D0–D8
DATA
BUFFER
INT 1
INTERRUPT
ARBITRATION
LOGIC
EN7
BUS
ARBITRATION
LOGIC

FIG: 1

3.0 SPECIFICATIONS

Word Size - 8 bits data BUS
Instruction: 8, 16, 24, 32 bits

Clock Period (T state): 250 nsec.

Memory capacity:

On board EPROMS up to 8K bytes
On board RAMS up to 4K bytes
Off board expansion up to 64K bytes, with user-specified combination of RAM, ROM, EPROM

Memory mapping:

On board EPROMS: jumper selectable 2716 (2K bytes) or 2732 (4K bytes)

jumper selectable for any 4K boundary within 64K address field. If 2732 is used two 4K EPROMS can be mapped completely independent from each other within 64K address field.

On board RAMS: Jumper selectable for any 4K boundary within 64K address field.

Memory speed required:

EPROM: 2716 or 2732 Access time: 450 ns max.

RAM: dynamic or static 450 ns max.

I/O Addressing:

On board programmable timer:

Port Address (HEX)	-	CTC CHANNEL
7C		0
7D		1
7E		2
7F		3

I/O Capacity:

Up to 256 can be decoded off board. The four port addresses, (7C, 7D, 7E, 7F) are used for on board timer/counter and cannot be used for any off board peripherals.

Interrupts:

Multi-level with three vectoring modes. Interrupt request may originate from user specified I/O or from the on board CTC.

System clock:

Min. - 500 KHz Max. - 4 MHz

Power supply requirement:

+5V ±5% at 1.5A max.

4.0 INTERFACE:

All address, data and command signals are TTL compatible.

5.0 MATING CONNECTOR:

See Table 1

6.0 CARD DIMENSIONS:

Length - 6.5 inches, 16.51 cm
Heigth - 4.48 inches, 11.38 cm
Thickness - .062 inches, .158 cm
Component Height Above Board - 0.338", 0.858 cm

7.0 ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0^{o} to $55^{o}C$

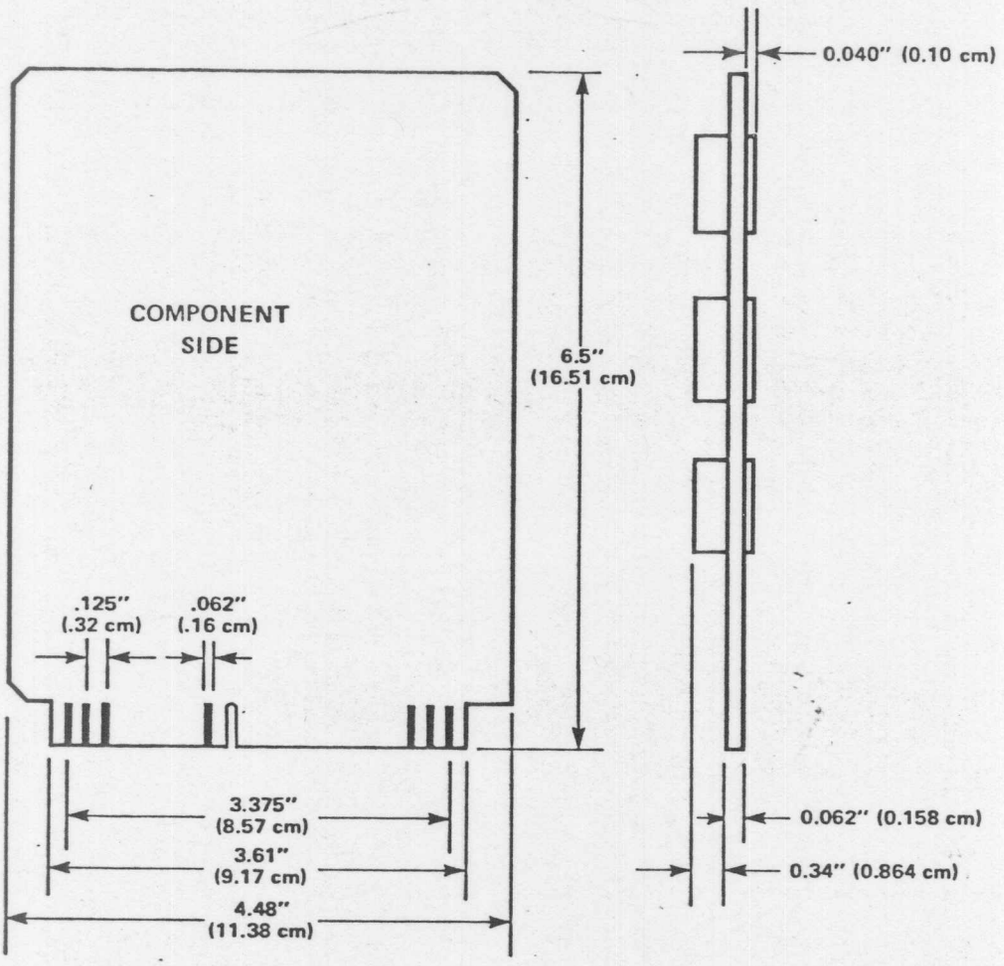
Storage Temperature: -40^{o} to $80^{o}C$

Relative Humidity: 0% to 90% without condensation

TABLE 1 - COMPATIBLE EDGE CONNECTORS

INTERFACE	NO. OF PAIRS/PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR P/N
STD BUS	28/56	0.125 In.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW28 DO-111
STD BUS	28/56	0.125 In.	Wire Wrap	Viking Winchester	VH28/ICHD5 HW28 DO-111

FIGURE 2 - STANDARD CARD OUTLINE



8.0 STD BUS ORGANIZATION AND FUNCTIONAL SPECIFICATIONS (WITH PIN DEFINITIONS)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1-6
Data Bus	Pins 7-14
Address Bus	Pins 15-30
Control Bus	Pins 31-52
Auxilliary Power Bus	Pins 53-56

TABLE 2 - STD BUS

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5	-5V	In	-5 Volts DC	6	-5V	In	-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP*	In/Out	I/O Expansion	36	MEMEX*	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
POWER BUS	53	AUXGND	In	AUX Ground (Bussed)	54	AUXGND	In	AUX Ground (Bussed)
	55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX-V.	In	AUX Negative (-12 Volts DC)

*Low Level Active Indicator

8.1 Data and Address Signals

8.1.1 Data Bus - Pins 7-14

An 8-Bit bidirectional 3-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read ($\overline{RD}$), Write ($\overline{WR}$) and interrupt Acknowledge ($\overline{INTAK}$).

The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ($\overline{BUSRQ}$) input from an alternate system controller, as in DMA transfers.

8.1.2 Address Bus - Pins 15-30

A 16-bit 3 state high-level active bus. The address will normally originate at the processor card. The processor card releases the Address Bus in response to a Bus Request ($\overline{BUSRQ}$) input from an alternate controller.

The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ($\overline{MEMRQ}$) and I/O request ($\overline{IORQ}$) control lines are used to distinguish between the two operations. The particular microprocessor used will determine the number of address lines and how they are used.

TABLE 3 - CONTROL SIGNAL FUNCTION

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{WR}$	PIN 31	Write to Memory or I/O - A 3-state, active low control line that indicates the BUS holds valid data to be written in the addressed memory or output device.
$\overline{RD}$	PIN 32	Read from Memory or I/O - A 3-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS.
$\overline{IORQ}$	PIN 33	I/O Address Select - A 3-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write.
$\overline{MEMRQ}$	PIN 34	Memory Address Select - A 3-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the address bus holds a valid address for memory read or memory write operations.
$\overline{IOEXP}$	PIN 35	I/O Expansion - An active-low control signal used to expand or enable I/O Port addressing. If this pin is not used, it is strapped to logic ground.
$\overline{MEMEX}$	PIN 36	Memory expansion - An active-low control signal used to expand or enable memory addressing. If this pin is not used, it is strapped to logic ground.
$\overline{REFRESH}$	PIN 37	A 3-state active-low control line used to refresh dynamic memory. The signal is generated on the processor card.
$\overline{MCSYNC}$	PIN 38	Machine Cycle Sync - A 3-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution). $\overline{MCSYNC}$ defines the beginning of the machine cycle.

TABLE 3 - CONTROL SIGNAL FUNCTION

CONTINUED

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{STATUS 1}}$	PIN 39	Status Control Line 1 - $\overline{\text{STATUS 1}}$ is a signal to identify instruction Fetch.
$\overline{\text{STATUS 0}}$	PIN 40	Status Control Line 0 - Status control line 0 is not generated on this processor card. $\overline{\text{HALT}}$ signal coming from processor could be strapped to this line.
$\overline{\text{BUSAK}}$	PIN 41	BUS Acknowledge - An active-low output line. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the BUS and giving an acknowledge signal on the $\overline{\text{BUSAK}}$ line. $\overline{\text{BUSAK}}$ occurs at the completion of the current machine cycle.
$\overline{\text{BUSRQ}}$	PIN 42	Bus Request - An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all 3-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed.
$\overline{\text{INTAK}}$	PIN 43	Interrupt Acknowledge - An active-low output line from the Processor card that occurs in response to ($\overline{\text{INTRQ}}$). It is used to tell the interrupting device that the processor card is ready to respond to the interrupt. For vectored interrupts, the vector address is placed on the data bus by the interrupting device during INTAK cycle.

TABLE 3 - CONTROL SIGNAL FUNCTION

CONTINUED

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{INTRQ}}$	PIN 44	Interrupt Request - An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the Processor unless deliberately enabled by a program instruction. If the Processor accepts the interrupt, it usually acknowledges by dropping $\overline{\text{INTAK}}$ (Pin 43).
$\overline{\text{WAITRQ}}$	PIN 45	Wait Request - An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a valid address on the address bus.
$\overline{\text{NMIRQ}}$	PIN 46	Non-Maskable Interrupt - An active-low processor card interrupt input line of highest priority.

TABLE 3 - CONTROL SIGNAL FUNCTION

(CONTINUED)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{SYSRESET}}$	PIN 47	System Reset - An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the bus that have latch circuits requiring initialization.
$\overline{\text{PBRESET}}$	PIN 48	Push Button Reset - An active-low input line to the system reset circuit.
$\overline{\text{CLOCK}}$	PIN 49	Clock from Processor - A buffered processor clock signal used for system synchronization or as a general clock source.
$\overline{\text{CNTRL}}$	PIN 50	An auxilliary circuit for special clock timing. It may be a multiple of the processor clock signal, a real time clock signal or an external clock input to the processor.
PCO	PIN 51	Priority chain output (output, active-high) this signal is sent to the PCI input of the next lower card in the priority chain.
PCI	PIN-52	Priority chain in (input, active-high). This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the processor card.

TABLE 4 - LOGIC POWER

• +5V	PINS 1 & 2	+5 Logic Voltage (VCC) Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
• GND	PINS 3 & 4	Logic Ground Ground for logic power. Both pins are bussed together for current capacity.

9.0 BOARD OPTIONS & UTILIZATIONS:

9.1 Memory Mapping (FIG: 3 and 4)

RAMS and EPROMS residing on CPU card can be mapped in 4K blocks independently anywhere within 64K address field.

		PAD
$\overline{EN1}$	= First 4K blocks of EPROM	E3
$\overline{EN2}$	= Second 4K block of EPROM	E11
$\overline{CSR}$	= 4K block or RAM	E4

Each one of the above 4K blocks can be independently moved within 64K address field in 4K increments. The pad designating the starting address for each 4K boundaries are as follows:

PAD	DESIGNATED STARTING ADDRESS
E2	0000H
E13	1000H
E14	2000H
E15	3000H
E16	4000H
E17	5000H
E18	6000H
E19	7000H
E20	8000H
E21	9000H
E22	A000H
E23	B000H
E24	C000H
E25	D000H
E1	E000H
E26	F000H

By jumpering the appropriate pads. $\overline{EN1}$, $\overline{EN2}$, $\overline{CSR}$ can be mapped independently.

RAM's can be enabled in 1K blocks through jumper straps (See FIG 4)
For 1K of on-board RAM: place E49 to E50,
For 2K of on-board RAM: place E49 to E50,
E51 to E52
For 3K of on-board RAM: place E49 to E50,
E51 to E52, E53 to E54
For 4K of on-board RAM: place E49 to E50,
E51 to E52, E53 to E54, E55 to E56.

NOTE: $\overline{EN2}$ is functional when 2732 (4K x 8) EPROM's are used, otherwise it has to be pulled high.

9.2.3 To start the CPU on power On, other than 0000H at the address not within on board memory range, but placed on another module within the STD Microcomputer System:

Place: E8 to E7
E9 to E10
Map the desired memory block by strapping them to their subsequent starting addresses (Note: EN1 should be strapped to where the power on jump should go).

Place the following instruction codes at the first 3 bytes of EPROM located at 4F.

C3 03 ( )

Power on starting address

Remove E6 to E7
E8 to E10

9.2.3 To start the CPU on power On, other than 0000H at the address not within on board memory range, but placed on another module within the STD Microcomputer System:

Place: E8 to E7
E9 to E10
Map the desired memory block by strapping them to their subsequent starting addresses (Note: EN1 should be strapped to where the power on jump should go).

Place the following instruction codes at the first 3 bytes of EPROM located at 4F.

C3 03 ( )

Power on starting address

Remove E6 to E7
E8 to E10

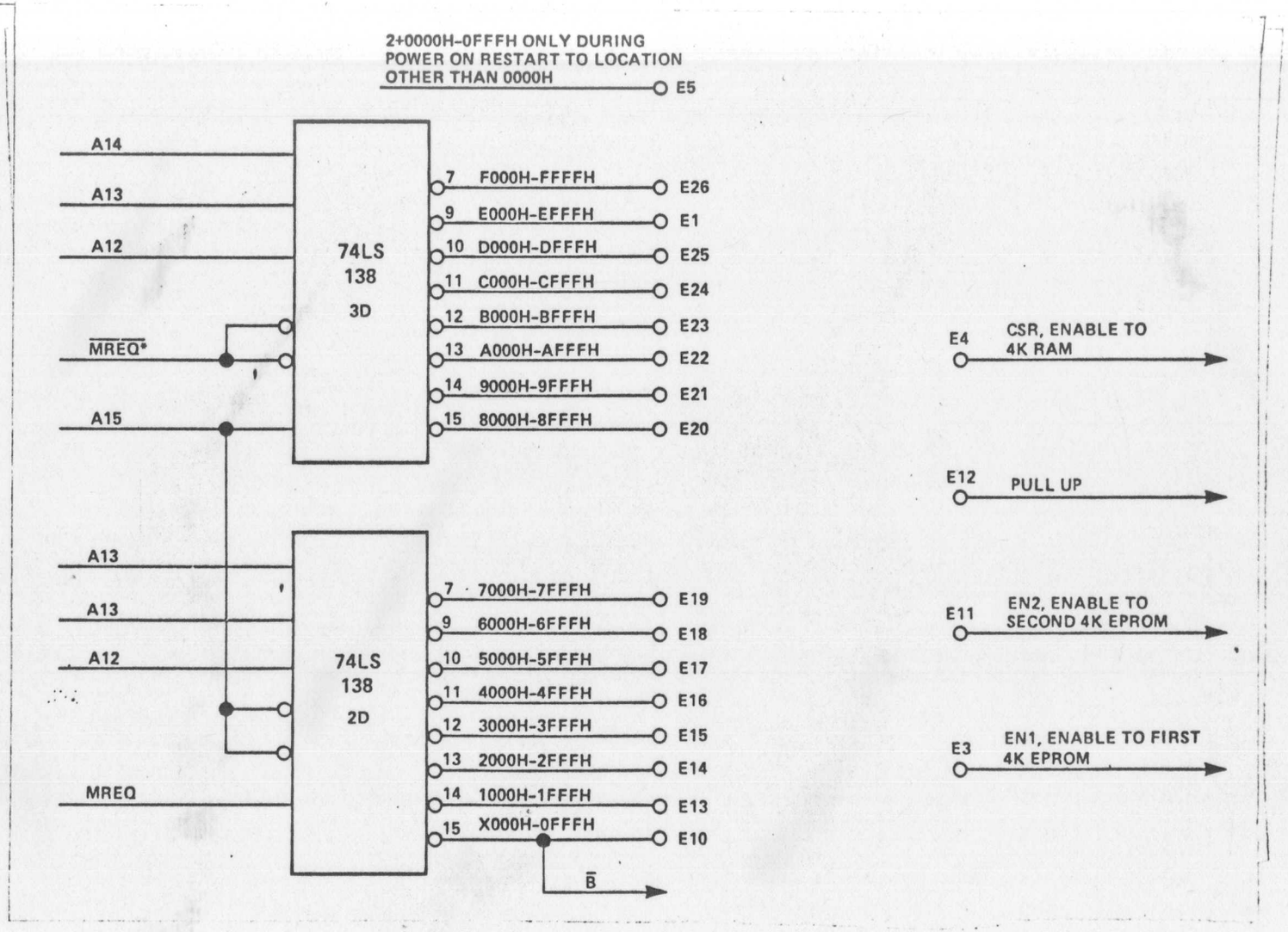
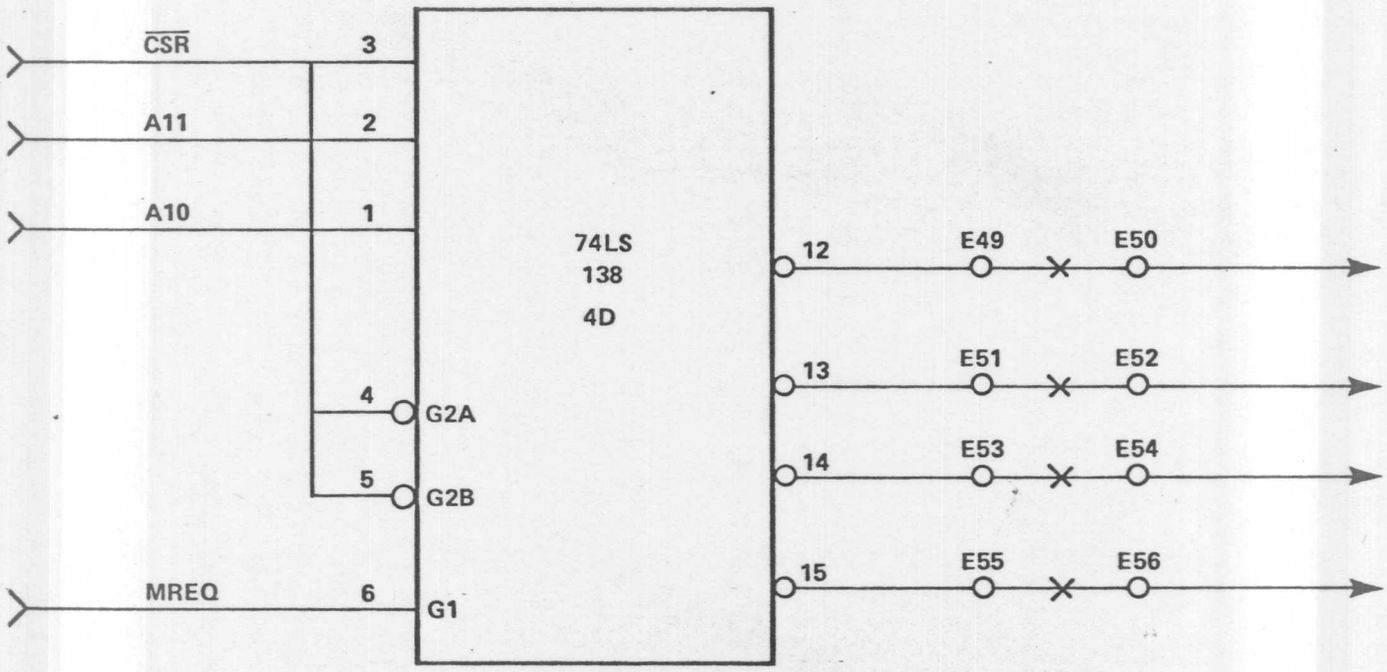

2+0000H-0FFFH ONLY DURING POWER ON RESTART TO LOCATION OTHER THAN 0000H
E5
A14
A13
A12
MREQ*
A15
74LS 138 3D
7 F000H-FFFFH E26
9 E000H-EFFFH E1
10 D000H-DFFFH E25
11 C000H-CFFFH E24
12 B000H-BFFFH E23
13 A000H-AFFFH E22
14 9000H-9FFFH E21
15 8000H-8FFFH E20
A13
A13
A12
MREQ
74LS 138 2D
7 7000H-7FFFH E19
9 6000H-6FFFH E18
10 5000H-5FFFH E17
11 4000H-4FFFH E16
12 3000H-3FFFH E15
13 2000H-2FFFH E14
14 1000H-1FFFH E13
15 X000H-0FFFH E10
B
E4 CSR, ENABLE TO 4K RAM
E12 PULL UP
E11 EN2, ENABLE TO SECOND 4K EPROM
E3 EN1, ENABLE TO FIRST 4K EPROM

FIG: 3

FIG: 4



Designate the printed circuit trace

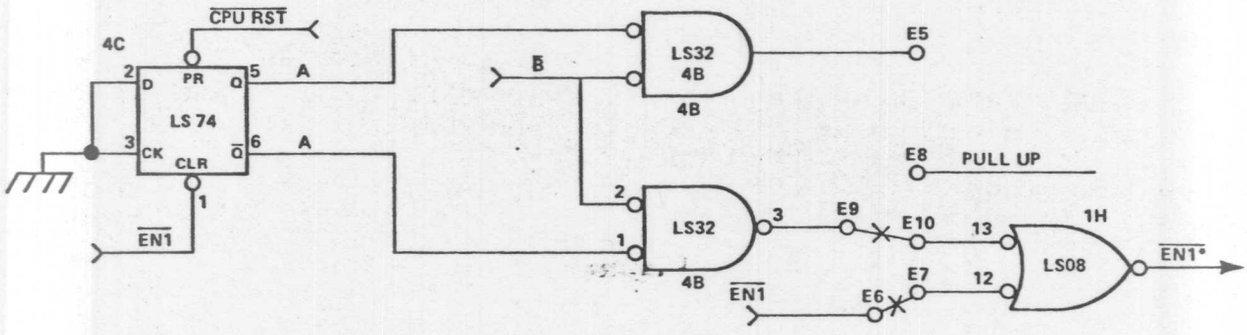


TABLE 9
FIG: 5

Designate the printed circuit trace.

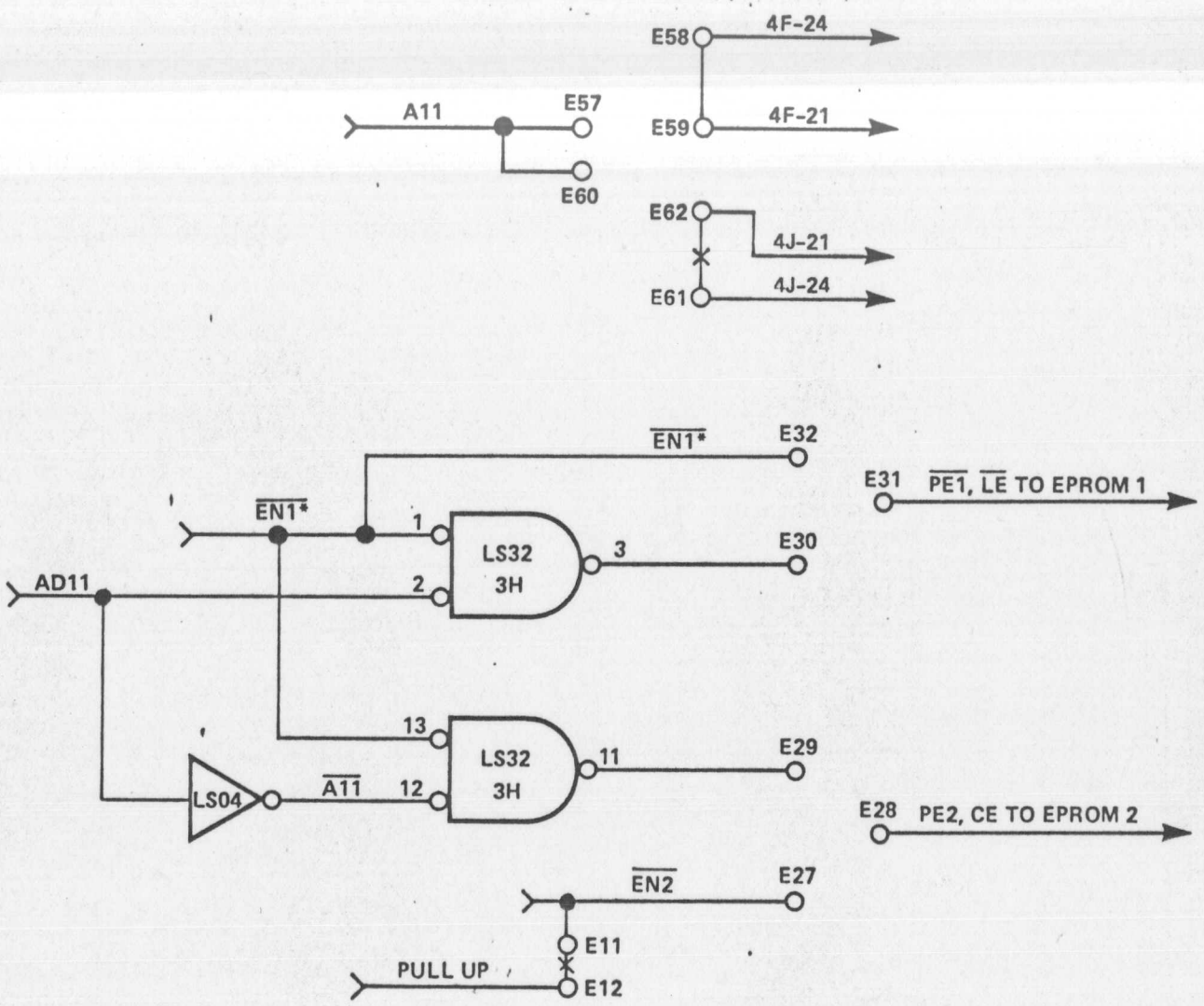


FIG: 6

Designate the printed circuit trace

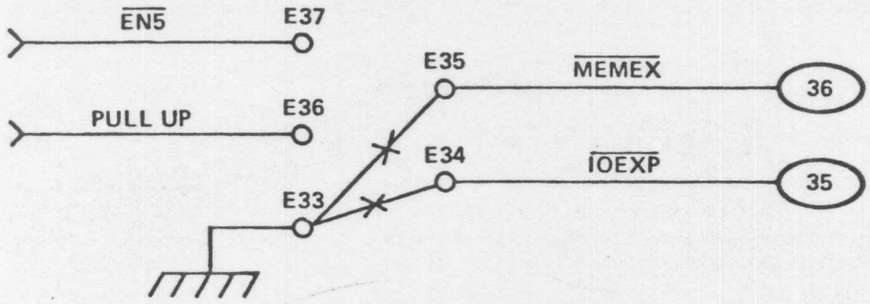


FIG: 7

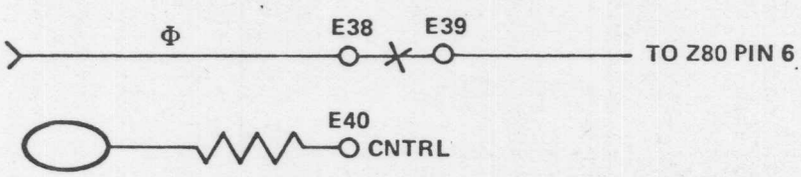


FIG: 8

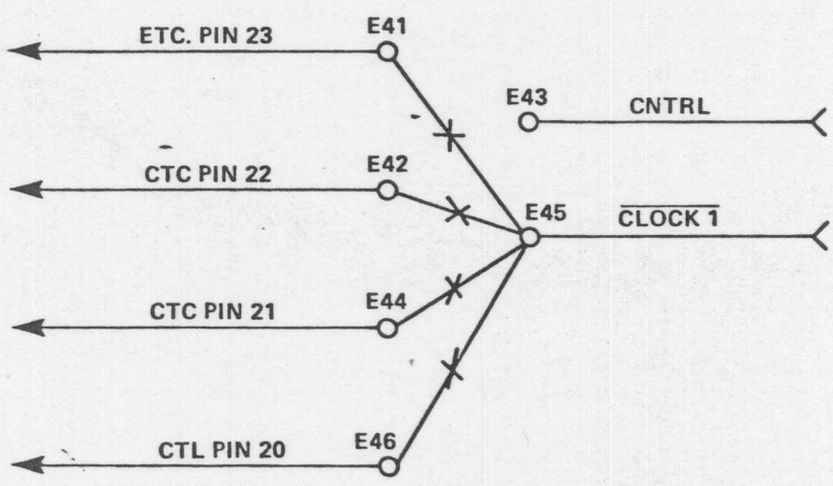


FIG: 9

10.0 DC CHARACTERISTICS

PARAMETER	LIMITS
Power V_{CC}	5V ±5% at 1.5A Max.
Operating Temperature	0 to 55° C
Input Loading	1 LS* Max.
Output Drive	60 LS* Loads Max.
Output 3-State Leakage	1 LS* Loads Max.

*Low-power Schottky.

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
Φ (A)	t_C	Clock Period	0.25	[12]	μs	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110		ns	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	ns	
	$t_{r,f}$	Clock Rise and Fall Time		30	ns	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	ns	
	$t_{F(AD)}$	Delay to Float		90	ns	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		ns	C_L = 50pF
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		ns	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MEMRQ}$	[3]		ns	Except T3, $\overline{ST1}$
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		ns	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	ns	
	$t_{F(D)}$	Delay to Float During Write Cycle		90	ns	
	$t_{S\Phi(D)}$	Data Setup Time to Falling Edge of Clock During $\overline{ST1}$ Cycle	50		ns	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge at Clock During M2 to M5	60		ns	C_L = 50pF
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		ns	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		ns	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		ns	
	t_H	Input Hold Time	0		ns	
$\overline{MEMRQ}$	$t_{DL\Phi(MR)}$	$\overline{MEMRQ}$ Delay From Rising Edge of Clock, $\overline{MEMRQ}$ Low	30	95	ns	
	$t_{DH\bar{\Phi}(MR)}$	$\overline{MEMRQ}$ Delay From Falling Edge of Clock, $\overline{MEMRQ}$ High		95	ns	
	$t_{DH\Phi(MR)}$	$\overline{MEMRQ}$ Delay From Rising Edge of Clock, $\overline{MEMRQ}$ High		95	ns	C_L = 50pF
	$t_{w(MRL)}$	Pulse Width $\overline{MEMRQ}$ Low	[8]		ns	
	$t_{W(MRH)}$	Pulse Width, $\overline{MEMRQ}$ High	[9]		ns	
$\overline{IORQ}$	$t_{DL\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		75	ns	
	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		85	ns	C_L = 50pF
	$t_{DH\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock $\overline{IORQ}$ High		85	ns	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	ns	
$\overline{RD}$	$t_{DL\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock $\overline{RD}$ Low		85	ns	
	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		95	ns	C_L = 50pF
	$t_{DH\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	ns	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	ns	
$\overline{WR}$	$t_{DL\bar{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		65	ns	
	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	ns	C_L = 50pF
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ High		80	ns	
	$t_{w(WRL)}$	Pulse Width, $\overline{WR}$ Low	[10]		ns	
$\overline{STATUS\ 1}$	$t_{DL(M1)}$	$\overline{ST1}$ Delay From Falling Edge of Clock, $\overline{ST1}$ Low		100	ns	C_L = 50pF
	$t_{DH(M1)}$	$\overline{ST1}$ Delay From Falling Edge of Clock, $\overline{ST1}$ High		100	ns	
$\overline{REFRESH}$	$t_{DL(RF)}$	Refresh Delay From Falling Edge of Clock, $\overline{REFRESH}$ Low		130	ns	C_L = 50pF
	$t_{DH(RF)}$	Refresh Delay From Falling Edge of Clock, $\overline{REFRESH}$ High		120	ns	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Rising Edge of Clock	70		ns	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Rising Edge of Clock		300	ns	C_L = 50pF
$\overline{INTRQ}$	$t_{s(IT)}$	$\overline{INTRQ}$ Setup Time to Falling Edge of Clock	80		ns	
$\overline{NMIRQ}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMIRQ}$ Low	80		ns	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Falling Edge of Clock	50		ns	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ Low		100	ns	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ High		100	ns	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Falling Edge of Clock (C)	60		ns	
	$t_{F(C)}$	Delay To/From Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	ns	
	t_{mr}	$\overline{STATUS1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		ns	

NOTE A. $\bar{\Phi}$ designates $\overline{CLOCK}$ on the STD BUS.

NOTE B. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{ST1}$ and $\overline{IORQ}$ are both active.

NOTE C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

[1] $t_{acm} = t_w(\Phi H) + t_f - 65$
[2] $t_{aci} = t_c - 70$
[3] $t_{ca} = t_w(\Phi L) + t_r - 50$
[4] $t_{caf} = t_w(\Phi L) + t_r - 45$
[5] $t_{dcm} = t_c - 170$
[6] $t_{dci} = t_w(\Phi L) + t_r - 170$
[7] $t_{cdf} = t_w(\Phi L) + t_r - 70$
[8] $t_w(MRL) = t_c - 30$
[9] $t_w(MRH) = t_w(\Phi H) + t_f - 20$
[10] $t_w(WR) = t_c - 30$
[11] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$
[12] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

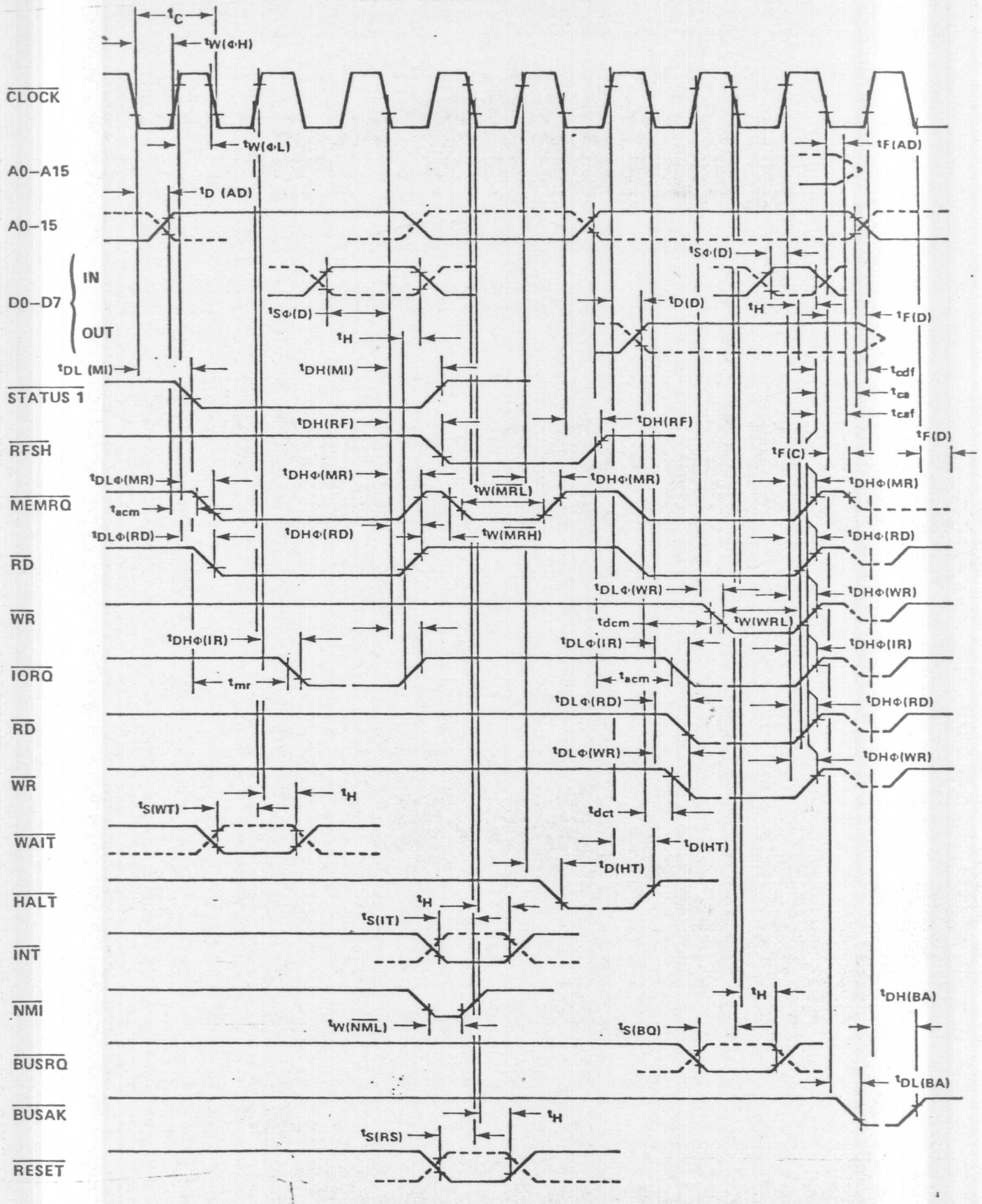


FIGURE 2. ISB-3100 Timing Diagram

12.0 ORDERING INFORMATION:

ORDERING PART NO.	DESCRIPTION
ISB-3100-01	4K Bytes of RAMs strapped to start a 2000_H Two EPROM sockets strapped to start at 0000_H
ISB-3100-02	No internal RAMs, one EPROM supplied with first 3 bytes programmed to power-on start the CPU at location $E000_H$
ISB-3100-03	One EPROM with first 3 Bytes programmed to power-on start the CPU at $E000_H$. 2K Bytes of RAMs mapped at $E800_H$.
ISB-3100-04	3K Bytes of RAMs starting at 2000_H 2 EPROM sockets starting at 0000_H
ISB-3100-05	2K Bytes of RAMs starting at 2000_H 2 EPROM sockets starting at 0000_H
ISB-3100-06	1K Bytes of RAMs starting at 2000_H 2 EPROM sockets starting at 0000_H
ISB-3100-07	No RAMs 2 EPROM sockets starting at 0000_H

NOTE:

Two EPROM sockets are provided. The EPROMS with appropriate ODT or other kinds of executive or utility programs can be ordered separately.

9.3 EPROM 2716 (2K x 8) or 2732 (4K x 8) Selection (FIG: 6)
Either 2716 or 2732 can be selected by appropriate jumper straps.

To select 2716:

Place E30 to E31
E29 to E28
E11 to E12
E58 to E59
E61 to E62
Remove E32 to E31
E27 to E28
E59 to E57
E62 to E60

To Select 2732:

Place E32 to E31
E27 to E28
E59 to E57
E62 to E60
Remove
E30 to E31
E29 to E28
E58 to E59
E61 to E62
E11 to E12

9.4 MEMEX, IOEXP See Fig 7

$\overline{\text{MEMEX}}$ or $\overline{\text{IOEXP}}$ can be jumpered to ground (E33) to enable off board memory and I/O all the time; or it can be pulled high through E36 to disable any off board I/O or memory operation. They can also be strapped to E37 (STD Bus Buffer enable), to ensure during any on board I/O or memory operation, the external I/O or memories are disabled.

9.5 Internal/External Clock Selection

External or internal clocks can be disabled or enabled through appropriate jumpers shown in FIG. 8 and 9 for Z80 Processor of each timer/counter clock/trigger input.